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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,065	06/20/2003	Ming-Huei Shieh	AF01169/AMDP975US	5651
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AMIN & TUROCY, LLP 1900 EAST 9TH STREET, NATIONAL CITY CENTER 24TH FLOOR, CLEVELAND, OH 44114			NGUYEN, DANG T	
			ART UNIT	PAPER NUMBER
			2824	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/600,065

Applicant(s)

SHIEH ET AL.

Examiner

Dang T. Nguyen

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Amendment filed on 1/31/06.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 6-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input checked="" type="checkbox"/> Other: <u>Search history</u> . |

Response to Amendment

1. This office action is in response to Applicant's amendment received on 1/31/06.
2. Claims 1, 13, 17, 18, 21 and 24 have been amended. Claim 5 has been cancelled. Claims 1 - 4 and 6 - 27 are pending on this application. Claims 1, 13, 17 and 24 are independent claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-4 and 6-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Independent claim 1, as amended, recites that "the plurality of multi-bit reference cells each associated with separate wordlines within the multi-bit memory core." There is no support for the recitation that each multi-bit reference cell is associated with a separate wordline within the multi-bit memory core. As described and especially as shown in Fig. 8 of the application, while the multi-bit reference cells (10) located in each column of the multi-bit array are each connected to a separate wordline, on each row of the array, these cells are connected to the same wordline. As such, the original disclosure does not provide support for the claim

language limiting each of the plurality of multi-bit reference cells to be associated with a separate wordline.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4 and 6-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, it cannot be ascertained whether the recitation "the plurality of multi-bit reference cells each associated with separate wordlines within the multi-bit memory core" limits each and every multi-bit reference cell to be associated with a separate wordline or does it limit each pair of reference cells (first and second reference cells) used to arrive at the reference voltage employed during data cell read operation to be connected to separate wordlines.

Regarding claim 13, line 7, the limitation "the plurality of reference pairs" lacks clear antecedent basis. It cannot be ascertained whether these pairs are reference cells that are the same or different from the multi-bit reference cells set forth earlier in the claim.

Claim 17, line 6, the limitation "the plurality of reference pairs" lacks clear antecedent basis and is indefinite for the same reason set forth for claim 13.

Claims 2-4, 6-12, 14-16 and 18-23 depend from an indefinite independent claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 - 14, and 17 – 26, as can be understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Le et al. U.S. Patent No. US 6,690,602 B1 - filed Apr. 8, 2002.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Claim 1 contains languages that are indefinite as indicated above. For examination purposes, the limitation “the plurality of multi-bit reference cells each associated with separate wordlines within the multi-bit memory core” is interpreted as limiting the first and second reference cells used in arriving at the reference voltage to be associated with separate wordlines within the multi-bit memory core. This

interpretation is deemed consistent with the disclosed invention (see especially Fig. 8 and its description).

Regarding independent claim 1, Fig. 3 of Lee et al. discloses an architecture that facilitates a reference voltage in a multi-bit memory [302], comprising: a multi-bit memory core [302] including a plurality of data cells [10] for storing data; first and second reference arrays [Dynamic Reference A, Dynamic Reference B] of a plurality of multi-bit reference cells [10's of Reference A, 10's of Reference B] (Col. 5 lines line 45), the first and second reference arrays [Reference A and Reference B] fabricated on the memory core (Fig. 3 [302]), the plurality of multi-bit reference cells [10's] each associated with separate wordlines [WL0 – WLn] within the multi-bit memory core (Col. 5 lines 44-50); and a first bit value of a first reference cell (Fig. 4 [414]) of the first reference array (Fig. 4 [Ref A]) averaged with a second bit value of a second reference cell (Fig. 4 [418]) of the second reference array (Fig. 4 [Ref B]) to arrive at the reference voltage (Fig. 4 $(A+B)/2$) employed during a data cell read operation (Col. 4, lines 15 – 17).

Regarding dependent claims 2 and 18, Fig. 3 of Le et al. discloses that the core further comprise a sector [Sector 1] of multi-bit data cells [10] organized in rows and columns with associated word lines [WLs] attached to the multi-bit data cells [10] in a row and with associated bit lines [BLs] attached to the multi-bit data cells [10] in a column, the first and second reference cells [304, 306] forming a multi-bit reference pair (Fig. 4) that is programmed and erased with the multi-bit data cells [10] during programming and erase cycles (Col. 6 lines 7 - 21).

Regarding dependent claims 3 and 19, Fig. 3 of Le et al. discloses that the multi-bit reference pair [304, 306] is associated with a word in a word line [WL0], the multi-bit reference pair utilized during reading of bits of the word (Col. 4 lines 15 - 17).

Regarding dependent claims 4 and 20, Fig. 3 of Le et al. discloses that the multi-bit reference pair [304, 306] is associated with multi-bit data cells [10s] in a wordline [WL0], the multi-bit reference pair [304, 306] is utilized during reading of bits in the wordline (Col. 4 lines 15 – 17).

Regarding dependent claims 6 and 22, Fig. 3 of Le et al. further discloses that the multi-bit reference pair [304,306] is associated with multi-bit data cells [10s] in the sector (Sector 1), the multi-bit reference pair [304, 306] is utilized during reading of bits in the sector (Col. 4 lines 15 – 17).

Regarding dependent claims 7 and 23, Le et al. discloses that the memory core (Fig. 3) includes a plurality of data sectors (Col. 5 lines 40 - 42) that are accessible by the first and second reference arrays [304, 306], the first and second reference arrays [304, 306] are located centrally of the plurality of data sectors (Fig. 3 disclosing multiple sectors separates by a broken lines for each sector, and the broken line on the right side of the Reference B clearly teaches there is at least one more sector which located on the right side of 304 and 306).

Regarding dependent claim 8, Figs. 1–3 of Le et al. discloses an integrated circuit comprising the memory.

Regarding dependent claim 9, Fig. 3 of Le et al. discloses a memory core of a computer system.

Regarding dependent claim 10, Fig. 3 of Le et al. discloses an electronic device of a memory system.

Regarding dependent claims 11 and 25, Le et al. discloses the first and second reference arrays (Fig. 3 [304, 306]) including corresponding reference cells (Fig. 4 [404, 406]) that are interleaved among the data cells (Fig. 4 [402]).

Regarding dependent claims 12 and 26, Fig. 3 of Le et al. discloses the memory core further comprising a plurality of data sectors (Col. 5 lines 40 - 42) such that each data sector is associated with at least one of the first and second reference array [304, 306] of multi-bit reference cells [10s].

Regarding independent claim 13, (Figs. 3 and 4) of Le et al. disclose an architecture that facilitates a reference voltage (Fig. 4) in a multi-bit memory comprising: a multi-bit memory core (Fig. 3) for storing data, the memory core including two groups (Col. 5 lines 40 – 42) of data sectors (Fig. 3 [10s]); first and second reference arrays (Fig. 3 [304, 306]) of a plurality of multi-bit reference cells (REFERENCE A, B), the first and second reference arrays (Fig. 3 [304, 306]) fabricated on the memory core (Fig. 3) interstitial to the groups (Col. 5 lines 40 – 42) of data sectors (Fig. 3 [10s]), the plurality of the reference pairs [Reference A and Reference B] each associated with a disparate wordline [WL0 or WL1] within the two groups of data sectors (Col. 5 lines 44-52); and a first bit value (Fig. 4 [404]) of a first reference cell (Fig. 3 [304]) of the first reference array (Fig. 3 [10s of 304]) and a second bit value (Fig. 4 [406]) of a second reference cell (Fig. 3 [306]) of the second reference array (Fig. 3 [10s of 306]) forming a reference

pair whose respective bit values are averaged (Fig. 4 [$(A+B)/2$]) to arrive at the reference voltage for the read operation (Col. 4 lines 15-17).

Regarding dependent claim 14, Le et al. discloses the groups (Col. 5 lines 40 – 42) of data sectors read in an interleaved manner with a selected reference pair (Fig. 4, Col. 4 lines 15 - 17).

Regarding independent claim 17, Fig. 3 of Lee et al. discloses a method for providing a reference voltage in a multi-bit memory [302], comprising: receiving a multi-bit memory core [302] for storing data; providing first a and second reference arrays [Dynamic Reference A, Dynamic Reference B] of a plurality of multi-bit reference cells [10's of Reference A, 10's of Reference B], the first and second reference arrays fabricated on the memory core (Fig. 3); associating each of the plurality of multi-bit reference pairs [Reference A and Reference B] with separate wordlines [WL0 – WLM] within the memory core (Col. 5 lines 44-50); and a first bit value of a first reference cell (Fig. 4 [414]) of the first reference array (Fig. 4 [Ref A]) averaged with a second bit value of a second reference cell (Fig. 4 [418]) of the second reference array (Fig. 4 [Ref B]) to arrive at the reference voltage (Fig. 4 $(A+B)/2$) employed and facilitate during a data cell read operation (Col. 4, lines 15 – 17).

Regarding dependent claim 21, Fig. 3 of Le et al. discloses the method of claim 18, as discussed above, the associated multi-bit reference pair [304, 306] utilized during reading of bits in the corresponding word line (Col. 4 lines 15 – 17).

Regarding independent claim 24, Fig. 3 of Lee et al. discloses a system for providing a reference voltage in a multi-bit memory, comprising: means for providing a

multi-bit memory core [302] for storing data; means for providing first and second reference arrays [Dynamic Reference A, Dynamic Reference B] of a plurality of multi-bit reference cells [10's of Reference A, 10's of Reference B], the first and second reference arrays [Reference A and Reference B] fabricated on the memory core (Fig. 3); and means for averaging a first bit value of a first reference cell (Fig. 4 [414]) of the first reference array (Fig. 4 [Ref A]) averaged with a second bit value of a second reference cell (Fig. 4 [418]) of the second reference array (Fig. 4 [Ref B]) to arrive at the reference voltage (Fig. 4 $(A+B)/2$) to facilitate a read operation (Col. 4, lines 15 – 17); and means [Wordline Controller] for separately monitoring process variations at each wordline within the multi-bit memory core (Col. 5 lines 44-54).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 16 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. U.S. Patent No. 6,690,602 B1 in view of Kurihara et al., U.S. Patent No. US 6,791,880 B1 - filed May 6, 2003.

Regarding dependent claims 16 and 27, Le et al. as applied to claims 13 and 24 above, respectively, discloses every aspect of applicant's claimed invention except

for a redundancy array located at least one of proximate and adjacent to the groups of data sectors.

Fig. 5 of Kurihara discloses a redundancy [525] array located at least one of proximate and adjacent to the groups of data sectors.

Le and Kurihara are both related to multi-bit memory cells. In view of teaching of Kurihara, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Kurihara's redundancy into the memory core of Le for the purpose of providing optimum tracking of the reference memory cells and core memory cells (Col. 6 lines 8-9).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. U.S. Patent No. 6,690,602 B1 in view of Ferrant, Patent No. US 6,538,942 B2 - filed Jun. 18, 2001.

Regarding dependent claim 15, Le et al. as applied to claim 13 above discloses every aspect of applicant's claimed invention except for the first and second reference arrays being precharged before being averaged.

Ferrant discloses precharging a row of reference cells. Ferrant teaches that the use of precharge circuit for precharging the reference cells before a reading or comparing operation is well known in the memory art (as shown in col. 1 lines 47-49).

Le and Ferrant are both related to memory cells. In view of Ferrant, it would have been obvious to one having ordinary skill in the art at the time the invention was made to precharge the reference arrays of Le before averaging for the purpose of improving the accuracy of average operation.

Response to Arguments

5. Applicant's arguments 1/31/06 have been fully considered but they are not persuasive.

Under remarks, with respect to claims 1, 13, 17 and 24, applicant argued that Le et al. is silent regarding "the plurality of multi-bit reference cells each associated with separate wordlines within the multi-bit memory core; and a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array". Examiner respectfully disagrees for the following reasons:

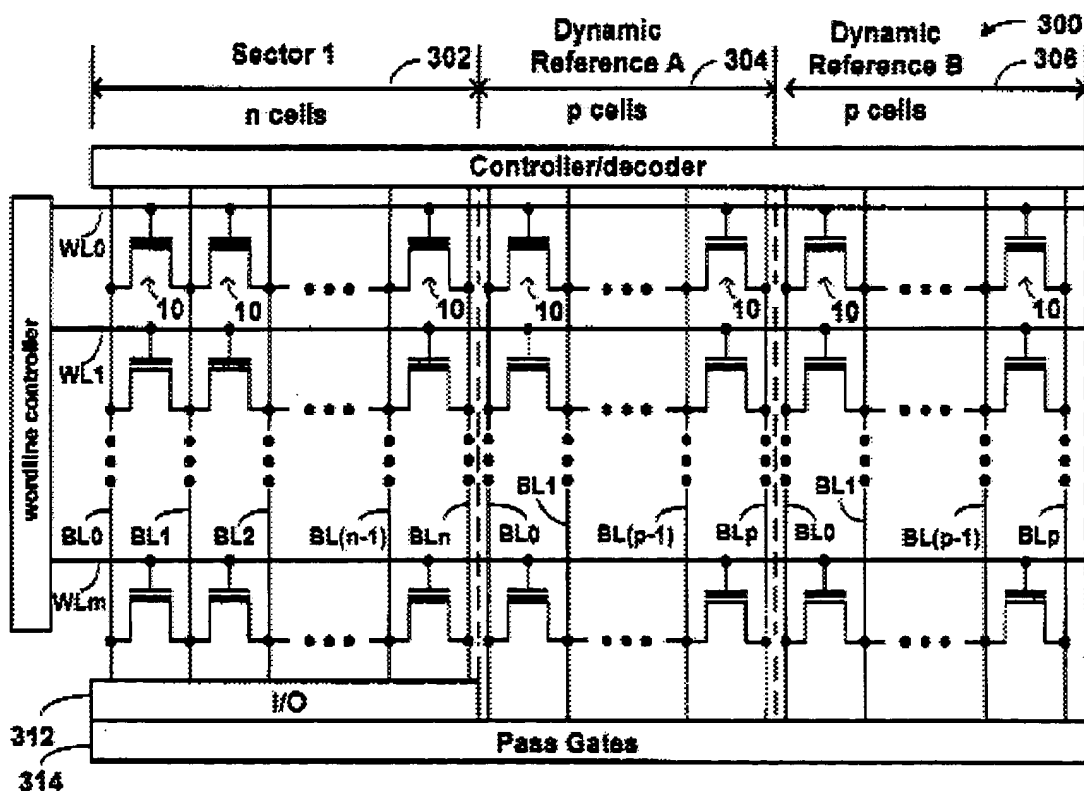


FIGURE 3

Fig. 3 of Le et al. discloses a plurality of multi-bit reference cells [cell 10s of Reference A and Reference B] each associated with separate wordlines WL0, WL1 to WLM within the multi-bit memory core (see Col. 5 lines 44-50); and

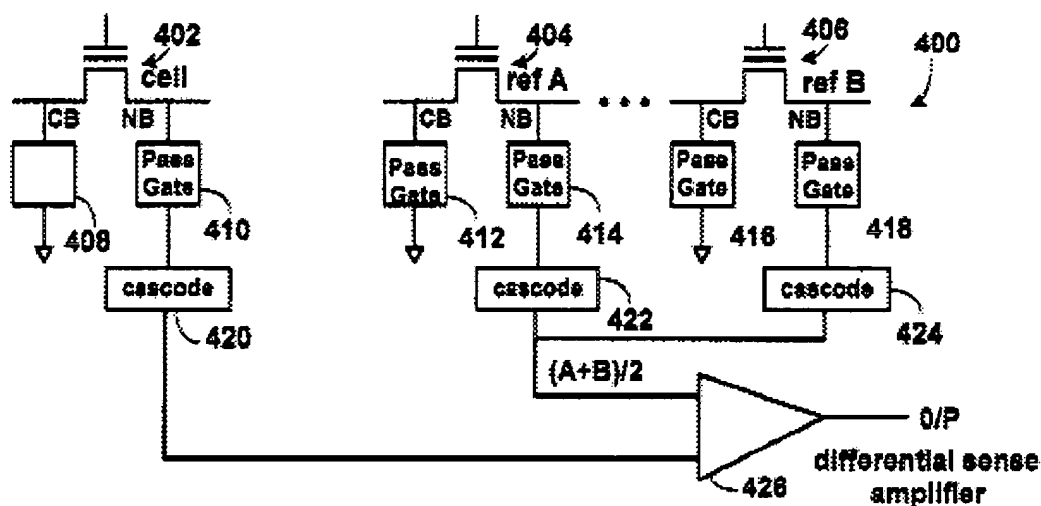


FIGURE 4

Fig. 4 of Le et al. clearly discloses a first bit value [414] of a first reference cell [404] of the first reference array [ref A] averaged $[(A+B)/2]$ with a second bit value [418] of a second reference cell [406] of the second reference array [ref B]. It is noted that Fig. 3 of Le et al. depicts the same structural configuration of the multi-bit memory core as that shown in Fig. 9 of the application.

It is argued that the prior art reference to Le et al. is silent about the novel aspects set forth in claims 1, 13, 17 and 24. Specifically, Le et al does not teach "the plurality of multi-bit reference cells each associated with separate wordlines within the multi-bit memory core; and a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage employed during a data cell read

operation.” (page 7, last full paragraph). However, as indicated in the rejections above, the recitation of a multi-bit reference cells each associated with separate wordlines in claim 1 finds no support in the original disclosure. Further, it is noted independent claims 13, 17 and 24 do not recite the argued limitation.

As claim 1 can be understood, and given its broadest reasonable interpretation consistent with the specification, it is anticipated by Le et al. While independent claim 1 recites that the plurality of the multi-bit reference cells each associated with separate wordlines within the multi-bit memory core, the claim language, even if supported by the original disclosure, does not exclude multiple multi-reference cells on the same row as shown in Fig. 3 of Le et al. to share the same wordline. The multiple multi-reference cells in each column of Fig. 3 of Le et al. are each associated with separate wordlines within the multi-bit memory core. Using the broadest reasonable interpretation standard, independent claim 1 is not deemed patentable over Le et al.

Regarding independent claims 13, 17 and 24, they are not deemed patentable for the reasons stated in the rejections above.

Regarding the dependent claims, it is argued that these claims are patentable by virtue of their dependence from a patentable independent claim. These arguments are not found to be persuasive since the independent claims are deemed unpatentable for the reasons indicated above. No separate argument for patentability for each dependent claim is presented by the applicant.

For the above-stated reasons, the rejection of claims 1, 13, 17 and 24 as being anticipated by Le et al. is believed to be proper. The dependent claims are deemed unpatentable for the reasons set forth in the rejections above.

Prior art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Van Buskirk et al. Pub. No.: US 2003/0208663 A1 Pub. Date: Nov. 6, 2003

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Contact Information

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 3/20/2006

 3/21/06

TUAN T. NGUYEN
PRIMARY EXAMINER